PHYSICS 536
Experiment 9: Common Emitter Amplifier

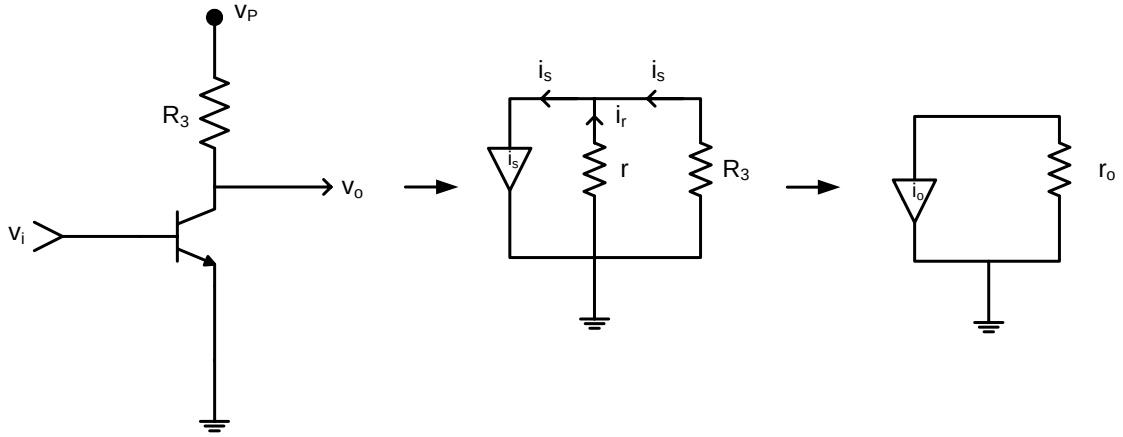
A. Introduction

A common-emitter voltage amplifier will be studied in this experiment. You will investigate the factors that control the midfrequency gain and the low-and high-break frequencies. Although a common-emitter amplifier is in principle a simple device it nevertheless utilizes a number of discrete components for proper operation. Below is a summary of the individual components and their purpose, and the symbol convention.

1) R_s is the output resistance of signal source.
2) C_2 is a "coupling capacitor" which passes AC signal from the source to amplifier input but blocks DC offsets from the source so that it does not affect the quiescent condition of the transistor.
3) C_3 is a coupling capacitor, which passes the amplified AC signal while preventing oscillations in the external load (R_L) from affecting the DC conditions.
4) R_2 fixes the DC potential at Base. The voltage drop across R_2 usually will be extremely small for a FET, but can be substantial for a BJT. The polarity of base voltage (I_bR_2) will be the same as the bias voltage V_n.
5) R_1 determines the quiescent current flowing through the transistor.
6) C_1 is a "by-pass" capacitor. It acts like a wire to connect emitter to common for all frequencies of interest.
7) R_3 is "load" resistor, which connects collector to power supply so that an output voltage can be created by changing the current through the transistor.

To determine the biasing conditions needed to obtain a specific gain each stage must be considered.

Step 1: A transistor can be represented as an ideal current source with an equivalent



resistor r in parallel. R_3 is the collector resistor for a BJT and the drain resistor for a FET. The output voltage is given by $v_o=-i_3R_3$. The minus sign occurs because the change in current always produces a voltage change at collector that is opposite to the input voltage change.

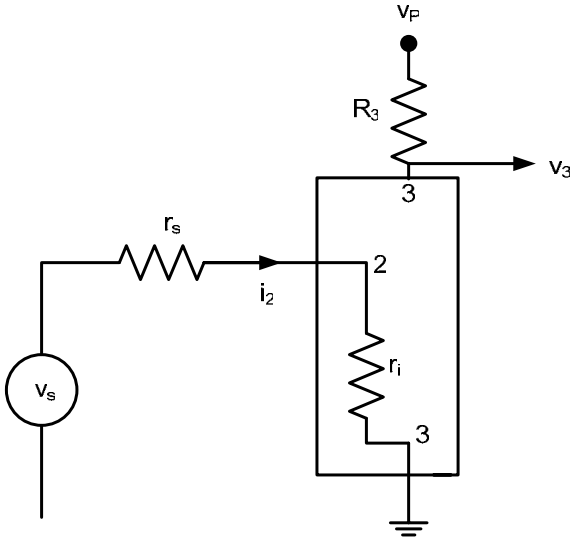
The voltage gain is given by $\frac{v_o}{v_i} = -A = -\frac{(r_3 \,||\, R_3)}{r_m}$.

r_m can be calculated by Ebers-Moll equation

$$r_m = \frac{25(\Omega - mA)}{I_C} + I\Omega$$

Step 2

The signal amplitude from a source depends on the current that the source must provide.



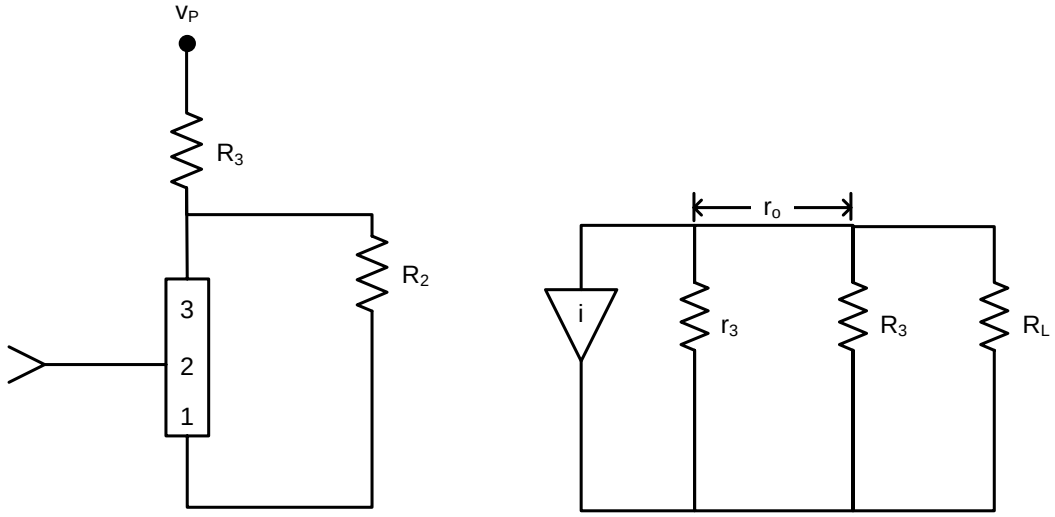
r_i is equivalent resistance of source. r_i specifies the current that flows in to base. The equivalent circuit shows that a simple voltage divider relation can be used to calculate the decrease in signal amplitude.

$$v_2 = v_s \frac{r_i}{r_s + r_i}$$

$$\text{Gain } A = \frac{v_3}{v_s} = \frac{r_i}{r_s + r_i}\left(-\frac{r_o}{r_m}\right)$$

Step 3

Signals are amplified for a purpose, to be applied to some "load."



Since R_L is in parallel with R_3 and r_3 so gain would be modified as

$$A = -\frac{r_i}{r_s + r_i}\left(\frac{r_0, R_L}{r_m}\right) = -\frac{r_i}{r_s + r_s} \times \frac{r_o R_L}{r_o + R_L} \times \frac{1}{r_m}$$

$$A = -\frac{r_i}{r_s + r_i}\frac{r_0}{r_m}\frac{R_L}{r_o + R_L}$$

$$A = -\frac{r_i}{r_s + r_C}(-a)\frac{R_L}{r_0 + R_L}$$

We see that the signal V_S is attenuated at the input, inverted and amplified by the device with gain "a", and attenuated at the output by the effect of load. Clearly gain has three parts.

1) Input attenuation (voltage divider): $\frac{r_i}{r_s + r_i}$
2) Device gain $a = \frac{r_o}{r_m}$
3) Output attenuation (voltage divider): $\frac{R_L}{r_o + R_L}$

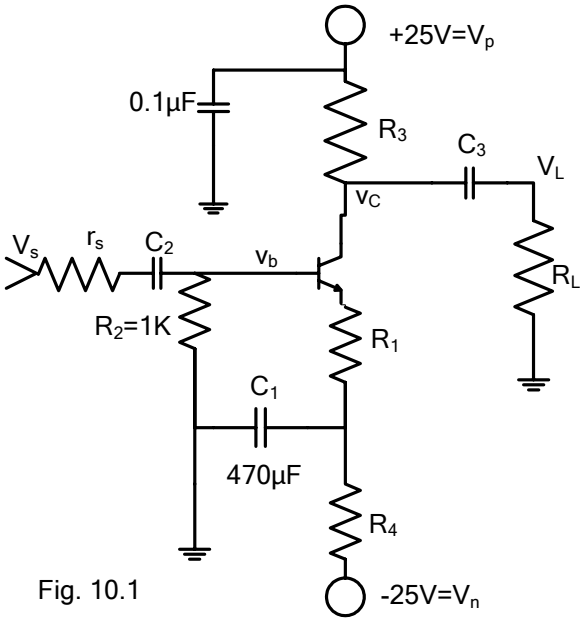


Fig. 10.1

1. For the circuit given in figure 10.1 the total gain is given by

$$A = \frac{v_L}{v_s} = \beta_{iL}\beta_{iH}\frac{R_{iT}}{r_s + R_{iT}}(a_m)\beta_{bL}\frac{R_L}{r_0 + R_L}\beta_{oL}\beta_{oH}$$

$\beta_{IH} < \beta_{OH}$ are higher frequency attenuation terms and $\beta_{iL} < \beta_{OL}$ are low frequency attenuation terms. So we can see that final gain expression has several components:

1) Device gain
2) Frequency independent input and output attenuation
3) Low frequency attenuation
4) High frequency attenuation

The mid-frequency gain of the transistor by itself is called the "device gain."

$$a_m = \frac{v_c}{v_b} = -\frac{r_o}{r_m + R_1}$$ (without the external load R_L resistor)

The input (R_{iT}) and output (r_o) resistance result in signal attenuation. The capacitors produce frequency dependent attenuation terms β that have the following form:

$$\beta_L = [1 + (f_L / f)^2]^{-1/2}$$

$$\beta_H = [1 + (f / f_H)^2]^{-1/2}$$

2. Break Frequencies: The coupling capacitors C_2 and C_3 cause low breaks at the input and output.

$$f_{iL} = [2\pi C_2 (r_s + R_{iT})]^{-1}$$

$$f_{oL} = [2\pi C_3 (r_o + R_L)]^{-1}$$

The by-pass capacitor C_1 at the emitter also causes a low break.

$$f_{bL} = [2\pi C_1 (r_m + R_1), R_4]^{-1}$$

Stray capacitance and capacitance inside of the transistors cause high breaks at the input and output.

$$f_{iH} = [2\pi C_i (r_s, R_{iT})]^{-1}$$

$$f_{oH} = [2\pi C_o (r_o, R_L)]^{-1}$$

Notice that the resistors are in series for the low breaks and in parallel for the high breaks.

3. BJT Parameters

$$r_m = \frac{25(\Omega - mA)}{I_c} + 1\Omega$$

$$r_o = (r_c, R_3)$$

$$r_c = 4000(r_m + R_1)$$

$$R_{iT} = (R_2, r_b)$$

$$r_b = h_{fe}(r_m + R_1)$$

4. FET Parameters

$$r_m = \frac{V_T}{2}\frac{1}{\sqrt{I_d I_{dss}}} \qquad r_o = (r_d, R_3)$$

$$r_d \approx 50K(\Omega - mA)/I_d$$

$$R_{iT} = R_2 \qquad (10.1)$$

$$V_{sg} = V_T(1 - \sqrt{I_d / I_{dss}})$$

5. Nonlinearity The I-V relation for transistors is nonlinear, hence the change in current is larger when V_{be} is increased rather than decreased.

$$\Delta I_c = I_2 - I_1 = I_1(e^{\Delta V_b / 25mV} - 1)$$

I_1 is the quiescent transistor-current.

MEASUREMENTS:

The same circuit will be used throughout the experiment, but the components will be changed to emphasize the various factors that affect the gain. Arrange the circuit similar to the diagram on page 1 to avoid confusion, and make it easy to change components. The resistance R_s is included to represent the effect of the signal-source resistance. In this representation the signal observed at point A is the "ideal v_s".

Component values are given at the back of these instructions. "D" indicates a direct connection in please of a component, and "X" means the component is not present.. The emitter resistor R_1 will be zero until step 18.

B. Midfrequency Gain and High-Frequency Attenuation

1) When referring to voltages refer use peak-to-peak voltages. V_s will be kept relatively small to minimize non-linearity. Monitor the input signal when the frequency is changed (refer to GIL section 4.3) For $I_c = 1mA$, measure the mid-frequency gain (v_c / v_b) at 10kHz. Observe that the gain is constant in the mid-frequency region by varying the signal frequency from 1kHz to 100kHz (i.e. the amplitude of V_c should be constant when V_b is constant). Measure the output high-break-frequency f_{oH} (refer to GIL sections 5.6, 5.6A). Measure the gain at 10 f_{oH}. Repeat the observations for $I_c = 5mA$. (You cannot observe the signal at $10\,f_{oH}$ for $I_c = 5mA$ because that is above the upper limit of the signal generator.)

Calculate the midfrequency gain and the output high-break frequency for I_c = 1 mA and 5 mA. The measured break frequencies may not agree with the calculated values from step 1, because that value depended on the assumed value of C_o (20 pF). However, the change in break frequency caused by the change in R_3 should agree with the calculation.

2) Calculate C_o from the measured f_{oH}. The scope probe used for the measurement adds about 10pf to C_o. The specifications for the 2N3904 estimates C_{bc} as 4pf. Estimate the stray capacitance (C_s) of your circuit from the measured C_o.($C_s = C_o - C_{bc} - C_{scope}$) C_s is relatively high in the plug-in chassis.

C. Input Attenuation at Mid- and High-Frequency

3) Use v_s =20mV. Measure the midfrequency gain v_c / v_s, and observe that it is constant from 1kHz to 50kHz.

4) Observe v_s and v_c and measure the break frequency introduced by C_i. Why is this measurement not affected by the output high-break-frequency?
Since $R_s = 0$ in the remainder of the experiment, there will be no high-frequency attenuation at the input.

D. Output Attenuation

5) Use v_s =20mV. Measure $A_m = v_L / v_s$, and observe that it is constant in the frequency range from approximately 1kHz to 100kHz.

E. Low Frequency Attenuation

The three low break frequencies will be investigated. Initially you will calculate all three frequencies to see which is dominant and check by measurement. Then the components will be changed to remove the higher breaks so that the lower breaks can be observed.

6) Use $v_s = 20mV$. Observe v_L to measure the low break frequency that marks the end of the midfrequency region (i.e. the highest of the three breaks).

7) Replace C_2 by a direct connection. Observe v_L to measure the middle low-break-frequency.

8) Remove C_3. Observe v_c top measure the lowest break frequency.

F. Transistor Nonlinearity

Transistor nonlinearity will be investigated in this part.

9) Connect the scope probe to the collector and use DC couplings at the scope input. Adjust the vertical position control so the trace (which represents the quiescent V_c) is in the center of the scope. Now apply input signals of 20, and 40mv (p-p) with f=10kHz. Measure the peak values of V_c relative to the quiescent line. The non-linearity should be very evident, but it may be smaller than calculated in step 14.

10) Increase v_s to observe the limits and compare to the calculations in 16. You should notice that you reach the negative limit first as indicated in calculation 14.

11) Measure a_m and compare.

You should also observe v_c with an amplitude of approximately 15V (p-p) to see that it is much more symmetric around the quiescent condition than it was in step 15. No report required.

G. Common-Source Amplifier

The BJT will be replaced by a FET in this section. The pin order is not the same for the two transistors (GI-10.1) V_{sg} is positive; hence the polarity of the source by-pass capacitor must be reversed.

12) Measure the quiescent voltage at the drain and source. Measure the device gain at 10kHz and observe that it is constant in the frequency range from 1kHz to 100kHz.

It should be evident that the gain potential of an FET is much smaller than it is for a BJT.

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Experiment 10: Components (A)

Assume η^{-1}=4000, D=Direct Connection, X=No Connection

Step	I_c	R_1	R_3	R_4	R_s	R_L	C_2	C_3
1-2	1	D	10K	24K	D	X	D	X
	5	D	2K	5.1K	D	X	D	X
3-4	5	D	2K	5.1K	2K	X	D	X
5	1	D	10K	24K	D	10K	D	0.01μf
6	1	D	10K	24K	D	10K	0.05μf	0.01μf
7	1	D	10K	24K	D	10K	D	0.01μf
8	1	D	10K	24K	D	X	D	X
9-10	1	D	10K	24K	D	X	D	X
11	1	240Ω	10K	24K	D	X	D	X
12	?	D	4.7K	10K	D	X	D	X

Initial Components

Transistor: 2N3904
Capacitors: 2 0.1 μf, 470 μf
Resistors: 1K, 10K, 24K

Please pick up the following components later if someone is waiting:

Transistor: MPF102
Capacitors: 0.01 μf, 0.05 μf
Resistors: 240Ω, 2 of 2 K, 4.7K, 5.1K, 10K